ABSTRACT OF THE DISCLOSURE

A circuit and method for boosting bitline performance uses a bitline booster circuit to allow long bitlines, with large numbers of memory cells attached, to discharge to a digital zero in a faster time. One bitline booster circuit requires only two additional NOR gates, two additional transistors, and one additional control signal. Consequently, the bitline booster circuit does not require a significant number of added components, does not require multiple control signals and takes up minimal additional silicon area.